



Rev. 04/03

174/212 Cont.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Chong H. Lee and Reza Asayesh  
Application No.: 10/643,276 Confirmation No.: 4060  
Filed : August 18, 2003  
For : PROGRAMMABLE LOGIC DEVICE WITH HIGH SPEED  
SERIAL INTERFACE CIRCUITRY  
Group Art Unit : 2819  
Examiner : Not yet assigned

New York, New York  
December 8, 2003

Hon. Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

TRANSMITTAL LETTER FOR  
INFORMATION DISCLOSURE STATEMENT

Sir:


Transmitted herewith is an Information Disclosure  
Statement in the above-identified application. This  
Statement is submitted:

- ☐ within three months of the application filing date;
- ☒ more than three months from the application filing date but before the mailing date of the first Office Action on the merits.

In accordance with 37 C.F.R. § 1.97, submission of  
this Statement requires no fee. However, if for any reason  
a fee is due, the Director is hereby authorized to charge

payment of any fees required in connection with this  
Information Disclosure Statement to Deposit Account  
No. 06-1075. A duplicate copy of this letter is transmitted  
herewith.

Respectfully submitted,




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I hereby certify that this  
Correspondence is being  
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Addressed to:  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450 on

  
December 8, 2003  
Claire J. Saintil van Goodman

  
Signature of Person Signing



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Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,  
applicants wish to call the attention of the Examiner to the  
following references:

U.S. patents	3,473,160	Wahlstrom
	4,486,739	Franaszek et al.
U.S. publication	20010033188-A1	Aung et al.

"Protocol Independent Gigabit Backplane Transceiver  
Using Lucent ORT4622/ORT8850 FPSCs", Application Note,  
June 2000, Lucent Technologies Inc., pp. 1-10.

"Lucent Introduces 10Gb/s Ethernet FPGAs,"  
Programmable Logic News & Views, Electronic Trend  
Publications, Inc., Vol. IX, No. 11, November 2000,  
pp. 7-8.

"ORCA ORT82G5 0.622/1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC", Product Brief, February 2001, Lucent Technologies Inc., pp. 1-8.

Virtex-II Pro Platform FPGA Handbook, UG012 (v1.0) January 31, 2002, Xilinx, Inc., pp. 1-6, 27-32, 121-126, and 162-180.

Rocket I/O Transceiver User Guide, UG024 (v1.2) February 25, 2002, Xilinx, Inc., pp. 1-106.

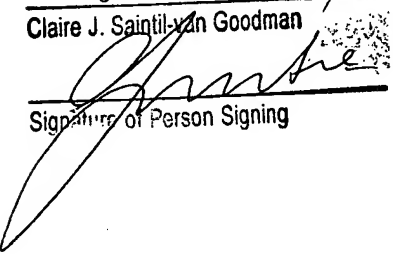
These references are also listed on the attached Form PTO-1449 (submitted in duplicate), and copies are enclosed.


Consideration of the foregoing in relation to this patent application is respectfully requested.

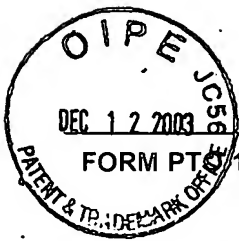
Respectfully submitted,

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Jared Kneitel  
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FORM PTO 1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE STATEMENT  
BY APPLICANTSDOCKET NO.  
174/212 Cont.APPLN. NO.  
10/643,276APPLICANTS  
Chong H. Lee et al.CONFIRMATION NO.  
4060FILING DATE  
August 18, 2003GROUP ART UNIT  
2819

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,473,160	10/14/69	Wahlstrom	326	41	
	4,486,739	12/04/84	Franaszek et al.	341	59	

## U.S. PUBLICATIONS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	2001/0033188 A1	10/25/01	Aung et al.	327	141	03/13/01

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
	"Protocol Independent Gigabit Backplane Transceiver Using Lucent ORT4622/ORT8850 FPSCs", Application Note, June 2000, Lucent Technologies Inc., pp. 1-10.
	"Lucent Introduces 10Gb/s Ethernet FPGAs", Programmable Logic News and Views, Electronic Trend Publications, Inc., Vol. IX, No. 11, November 2000, pp. 7-8.
	"ORCA ORT82G5 0.622/1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC", Product Brief, February 2001, Lucent Technologies Inc., pp. 1-8.
	Virtex-II Pro Platform FPGA Handbook, UG012 (v1.0) January 31, 2002, Xilinx, Inc., pp. 1-6, 27-32, 121-126, and 162-180.
	Rocket I/O Transceiver User Guide, UG024 (v1.2) February 25, 2002, Xilinx, Inc., pp. 1-106.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicants.